

REMARKS

Claims 6, 10-13, 15 and 16 are pending. Claims 15 and 16 have been allowed. Amendment of claims 6 and 10 is proposed. A marked-up version showing the proposed changes to claims 6 and 10 is attached hereto as “**Version with markings to show changes made.**”

Entry of the amendment after final rejection is earnestly solicited. It is respectfully submitted that the amendment places the application in condition for allowance.

Claims 10-12 were rejected under USC § 102(e) as being anticipated by *Arai et al.* Favorable reconsideration of this rejection is earnestly solicited.

Arai et al. teaches a process in which ion implantation of nitrogen is conducted obliquely at first, followed by an ion implantation process of As to form diffusion regions. According to such process, the nitrogen ion is introduced intentionally into the part of the gate oxide film located immediately underneath the gate electrode, while this is exactly what the present invention intends to avoid.

As shown in Fig. 4 of the present application, nitrogen is introduced into the gate oxide film in correspondence to the part near the drain edge while avoiding the region located underneath the gate electrode. By doing so, it becomes possible to terminate harmful dangling bonds in the gate oxide film near the drain edge while simultaneously avoiding the unwanted problem of shifting of the threshold characteristic of the MOS transistor.

Since the nitrogen ions are introduced in advance to the formation of the diffusion regions in *Arai et al.*, the nitrogen atoms cause diffusion, and while some may escape, some may penetrate deeply into the part of the gate oxide film located underneath the gate electrode. Thereby, a problem of shifting of threshold characteristic will be induced in the MOS transistor of *Arai et al.*

In the present invention as set forth in claim 10, the introduction of nitrogen is conducted after the step of formation of the diffusion regions. Thus, penetration of nitrogen atoms into the region of the gate oxide film right underneath the gate electrode is suppressed effectively and the problem of unwanted shifting of the threshold characteristic is successfully avoided.

In order to clarify the forgoing point of the present invention, amendment of claim 10 is proposed. With this amendment, the present invention is clearly distinguished over Arai.

Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over *Ito et al.* in view of *Maiti et al.* Favorable reconsideration of this rejection as earnestly solicited.

Again, it is noted that *Ito et al.* teaches the step of introduction of nitrogen prior to the step of forming diffusion regions. Thus, the nitrogen region 24 goes deeply into the region of the gate oxide film underneath the gate electrode with the formation of the impurity diffusion region as can be seen in Figs. 1D and 1E of *Ito et al.* Further, the process of *Ito et al.*, in which the nitrogen ions are introduced into the Si substrate at the lateral sides of the gate electrode (Fig. 1D of *Ito et al.*), causes the problem of extensive formation of N-H bonding and associated surface states.

With regard to *Maiti et al.*, it is noted that *Maiti et al.* is also silent about the feature of introducing nitrogen after the step of introducing the impurity elements. Thus, even when combined, the features of amended claim 6 is not derived.

In addition, it is noted that *Maiti et al.* teaches the process of forming a tunneling oxide film of a flash memory, while *Ito et al.* teaches the process of forming a MOS transistor. Thus, there is no motivation for a person skilled in the art to combine *Maiti et al.* and *Ito et al.*

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicant would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicant's undersigned attorney.

In the event that this paper is not timely filed, applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,
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Attachment: Version with markings to show changes made

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IN THE CLAIMS:

Claims 6 and 10 have been amended as follows:

6. (Three Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

forming diffusion regions in said substrate at both lateral sides of the gate electrode pattern by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

said step of introducing said impurity element being conducted prior to said step of introducing N atoms into said gate oxide film.

wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing NO,
wherein activation of said impurity element is conducted simultaneously to said thermal annealing process.

said thermal annealing process being conducted at a temperature of about 800°C.

10. (Four Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

forming diffusion regions in said substrate at both lateral sides of the gate electrode pattern by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms, after said step of introducing said impurity element, into said gate oxide film while using said gate electrode pattern as a mask,
wherein said step of introducing N atoms into said gate oxide film comprises the steps of conducting an ion implantation process of N ions; and applying a thermal annealing process to said gate oxide film.